WHAT IS CLAIMED IS:

1. A motor drive system, comprising:

a power inverter circuit including a plurality of power switches for applying electrical energy to the motor;

a power converter circuit coupled to the power inverter circuit for converting input power to a form usable by said power inverter circuit;

a power factor correction circuit in the power converter circuit for conditioning input current to cause the motor drive system to appear as a resistive load to the input power;

an active EMI filter coupled to at least one of the power converter and power inverter circuits for reducing EMI noise in the motor drive system;

a system controller coupled to the power converter circuit and power inverter circuit and operable to provide control signals to the power inverter and power converter circuits to coordinate switching between the power inverter and power converter circuits to reduce EMI noise production.

2. The motor drive system according to claim 1, further comprising a gate drive circuit coupled to the system controller and the power inverter circuit for providing drive signals to switches in the power inverter circuit based on control signals received from the system controller.

3. The motor drive system according to claim 2, further comprising a dv/dt command signal from the system controller to at least one of the power converter circuit and gate drive circuit for controlling a gate voltage rate of change per unit time for a specified switch.

4. The motor drive system according to claim 1, further comprising a feedback signal representative of the power usable by the power inverter circuit and coupled to the system controller for reconstructing an estimate of motor current.

5. The motor drive system according to claim 1, further comprising an algorithm executable by the system controller to influence system EMI noise, the algorithm being influenced by EMI noise related indicia to provide an adaptive closed loop EMI noise reduction.

6. A gate driver for a power switch, comprising:

a gate drive circuit coupled to the gate of the power switch for at least one of turning on and turning off the power switch;

a gate voltage control circuit in the gate drive circuit for controlling a voltage applied to the gate of the power switch during at least one of turning on and turning off the power switch; and

a signal supplied to the gate voltage control circuit indicative of a voltage rate of change per unit time to be applied in at least one of turning on and turning off the power switch.

7. The gate driver according to claim 6, further comprising a CMOS circuit coupled to the power switch and the gate voltage control circuit for supplying a control voltage to the power switch.

8. The gate driver according to claim 6, wherein the gate voltage control signal is an analog voltage signal.

9. The gate driver according to claim 6, further comprising a level shifting circuit for shifting a reference for the gate driver to a high voltage reference.

10. The gate driver according to claim 9, further comprising:

a variable pulse width generator coupled to the level shifting circuit and operable to provide the level shifting circuit with pulses indicative of a beginning and end of a gate command for the power switch; and

the pulses having a width that varies dependent upon a desired dv/dt control parameter.

11. The gate driver according to claim 9, further comprising a pulse consolidation circuit for producing a switch command based on a beginning and end pulse, the switch command being applied to control the gate of the power switch.

12. The gate driver according to claim 11, wherein the pulse consolidation circuit is an RS flip flop, with the beginning and end pulses coupled to inputs of the flip flop.

13. The gate driver according to claim 9, further comprising a pulse to voltage converter coupled to the level shifting circuit and operable to provide an analog voltage level based on a width of an input pulse, the analog voltage level being applied to the gate voltage control circuit.

14. A motor drive control for driving a motor, comprising:

a power switch coupled to the motor for switching electrical energy in the motor;

a dv/dt control coupled to a gate of the power switch for controlling a voltage rate of change per unit time for at least one of turning on and turning off the power switch;

a controller coupled to the dv/dt control and operable to provide commands to the dv/dt control to specify dv/dt operation;

an algorithm executable by the controller to reduce EMI noise production through the dv/dt control and reduction of switching losses in the power switch.

15. The motor drive control according to claim 14, further comprising a reduced dv/dt based on execution of the algorithm for a turn on time of the power switch.

16. The motor drive control according to claim 14, further comprising reduced dv/dt based on execution of the algorithm for at least one of a turn on and turn off time for the power switch.

17. The motor drive according to claim 15, wherein the dv/dt control reduces differential mode noise.

18. The motor drive control according to claim 16, wherein the dv/dt control reduces common mode noise.

19. A noise extraction circuit for a closed loop motor drive control, comprising:

a noise energy extractor operable to sense a noise signal and determine an energy indicia of energy contained in the noise signal;

a noise synchronization circuit coupled to the noise energy extractor and operable to determine a timing indicia related to the noise signal; and

a converter coupled to the noise synchronization circuit for translating the timing and energy indicia into a digital device readable format, whereby a digital device can receive information related to the noise signal.

20. A motor drive control system for driving a motor, comprising:

a power inverter circuit coupled to the motor;

a power converter circuit coupled to the power inverter for supplying power usable by the power inverter circuit;

a controller coupled to the power converter and the power inverter circuits to control operation of the power converter and power inverter circuits;

a noise feedback signal supplied to the controller for operating the motor drive control system with reduced noise, wherein the noise feedback signal is supplied by the circuit according to claim 19.

21. A method for reducing noise in a motor drive system, comprising:

sensing noise in at least an input section of the motor drive system;

supplying the sensed noise to a motor drive system controller;

adaptively controlling at least one of a power converter and power inverter based on the sensed noise to reduce noise in the motor drive system.

22. The method according to claim 21, further comprising:

synchronizing switching between the power inverter and power converter to reduce EMI noise.

23. The method according to claim 21, further comprising:

supplying a signal to a power switch gate drive in at least one of the power converter and the power inverter; and

controlling the gate drive to produce a specified voltage rate of change per unit time for at least one of turning on and turning off the power switch based on the supplied signal.

24. The method according to claim 23, further comprising converting the supplied signal to a level shifted pulse sequence applied to the gate drive.

25. The method according to claim 24, further comprising determining a specified voltage rate of change per unit time based on a width of the level shifted pulses.

26. A method for controlling a motor drive system to reduce noise, comprising:

providing a signal related to a desired voltage rate of change per unit time for a gate of a power switch in the motor drive system;

applying the signal to a gate driver for the power switch;

varying the power switch turn on or turn off time based on the signal; and

modifying the signal based on an adaptive trade off between noise reduction and switching losses in the power switch by changing turn on or turn off times of the power switch.

27. The method according to claim 26, further comprising applying a slow voltage rate of change per unit time to turn on the power switch to reduce differential mode noise.

28. The method according to claim 26, further comprising applying a slow voltage rate of change per unit time to turn on and turn off the power switch to reduce common mode noise.

29. A method for sensing noise in a motor drive control system, comprising:

obtaining a noise energy indication from a noise signal;

obtaining a synchronized noise signal related to the indication;

converting the synchronized noise signal to a digitized machine readable format; and

providing the converted signal to a digital numerical computational device.

30. The method according to claim 29, further comprising providing control signals from the computing device to operate the motor drive control system to reduce noise based on information related to the noise signal.

31. An integrated circuit for supplying gate command signals to a power switch, comprising:

a gate drive output for applying turn on and turn off signals to the power switch;

a gate drive command input for providing command signals to operate the gate drive output;

a voltage rate of change per unit time signal input for controlling the gate drive output to produce a specified voltage applied to the gate of the power switch during turn on or turn off times; and

a gate voltage control circuit coupled to the voltage rate of change per unit time signal and the gate drive output, the voltage rate of change per unit time signal

influencing the gate voltage control circuit to control the voltage applied to the gate control output in conjunction with the gate command signal for turning on or turning off the power switch.

32. The integrated circuit according to claim 31, further comprising:

a second gate drive circuit for providing an output to control a gate of a second power switch;

a second gate command signal input to control the second gate drive circuit;

a second voltage rate of change per unit time signal input coupled to the second gate drive circuit for controlling a voltage rate of change per unit time for the output provided by the second gate drive circuit; and

a level shifting circuit coupled to the second gate command signal input and the second gate drive circuit for shifting a voltage level of the second gate command signal input.